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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,375	10/16/2001	Yoshinobu Ono	2185-0578P	3053

2292 7590 06/18/2003

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EXAMINER

IM, JUNGHWA M

ART UNIT PAPER NUMBER

2811

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/977,375

Applicant(s)

ONO ET AL.

Examiner

Junghwa M. Im

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 January 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,5-11,14 and 15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,5-11 and 15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 6-11 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Mishima et al. (U.S. Pat. No. 5,633,516), hereafter Mishima in view of Udagawa et al. (U.S. Pat. No. 6,462,361), hereafter Udagawa and Kizuki (U.S. Pat. No. 5,948,161)

Regarding claims 1 and 11, Fig. 1 of Mishima shows a 3-5 group compound semiconductor comprising a GaAs substrate (1), a buffer layer (2) on said GaAs substrate and an epitaxial crystal layer (5) on said buffer layer, and said layers being formed by an epitaxial crystal growth method, wherein said buffer layer and said epitaxial crystal layer on said buffer layer are 3-5 group compound semiconductors each independently represented by the general formula $\text{In}_x\text{Ga}_y\text{Al}_z\text{As}$ (wherein, $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$, $x + y + z = 1$) (col.3, lines 26-52 and col.4, lines 28-34).

Mishima fails to teach that wherein the buffer layer has a structure of n times ($1 \leq n \leq 30$) of $\text{Ga}_{1-z}\text{Al}_z\text{As}$ (wherein, $0 < z \leq 1$) layer and GaAs layer. Fig. 1 of Udagawa teaches a superlattice structured buffer layer (11) of AlGaAs/GaAs on a GaAs substrate (10). Also note a respective of specification especially col. 4, lines 19-22.

It would have been obvious to one of ordinary skill in the art at the time of

the invention was made to incorporate the teaching of Udagawa into the device taught by Mishima since the heterojunction structure of the buffer layer absorbs the dislocation gradually and improves the performance of the device.

The device of Mishima and Udagawa shows substantially the entire claimed structure except the dislocation density in the epitaxial crystal layer being $2000/\text{cm}^2$ or less. Kizuki teaches that a semiconductor device of GaAs substrate having the dislocation density of the crystal layer reduced to 1×10^3 (col. 11, lines 3-13). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Kizuki into the device taught by Mishima and Udagawa since the device breakdown can be alleviated through the reduction of the defect density and resulting lattice-misfit.

Regarding claim 6, Mishima shows that at least one layer of two kinds of layers in the buffer layer is doped with an n-type dopant (col. 5, line 22 and col.4, lines 28-34).

Regarding claim 7, Mishima shows that said n-type dopant is Si and the concentration of the Si is $1 \times 10^{17} \text{ cm}^{-3}$ or less (col.5, lines 43-45).

Regarding claims 8 –10, Mishima shows that the buffer layer is doped with n type Si dopant as discussed above in claims 6 and 7. Regarding the planar doping concentration, Mishima teaches the concentration of Si in terms of volume as discussed in claim 7, while the instant claim recites the identical concentration range in term of surface area.

Claims 2 and 5 are rejected under 35 U.S.C. 103 (a) as being unpatentable

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over Mishima in view of Udagawa and Inoue (U.S.Pat. No.5,134,446).

Regarding claim 2, Fig. 1 of Mishima shows a 3-5 group compound semiconductor comprising a GaAs substrate (1), a buffer layer (2) on said GaAs substrate and an epitaxial crystal layer (5) on said buffer layer, and said layers being formed by an epitaxial crystal growth method, wherein said buffer layer and said epitaxial crystal layer on said buffer layer are 3-5 group compound semiconductors each independently represented by the general formula $\text{In}_x\text{Ga}_y\text{Al}_z\text{As}$ (wherein, $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$, $x + y + z = 1$) (col.3, lines 26-52 and col.4, lines 28-34).

Mishima fails to teach that wherein the buffer layer has a structure of n times ($1 \leq n \leq 30$) of $\text{Ga}_{1-z}\text{Al}_z\text{As}$ (wherein, $0 < z \leq 1$) layer and GaAs layer. Fig. 1 of Udagawa teaches a superlattice structured buffer layer (11) of AlGaAs/GaAs on a GaAs substrate (10). Also note a respective of specification especially col. 4, lines 19-22.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Udagawa into the device taught by Mishima since the heterojunction structure of the buffer layer absorbs the dislocation gradually and improves the performance of the device.

The device of Mishima and Udagawa shows substantially the entire claimed structure except the dislocation density in the epitaxial crystal layer on the buffer layer is $1/3$ or less of the dislocation density in the GaAs substrate. Inoue shows that the dislocation density of the crystal layer on the buffer layer is $1/3$ or less of the dislocation density of the substrate through following example. In col.1, lines 44-48, Inoue discloses the GaAs substrate with a dislocation density of $10^{12} / \text{cm}^2$. And Inoue discloses, in col.

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5, lines 8-18, the dislocation density of the crystal layer on the buffer layer can be reduced to about $1 \times 10^6/\text{cm}^2$. Therefore, the dislocation density in the epitaxial crystal layer is less than $1/3$. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Inoue into the device taught by Udagawa to make the dislocation density being less than $1/3$ in order to reduce the defect density and resulting lattice-misfit.

Regarding claim 5, Inoue teaches that the value of z in one of the buffer layers ($\text{Ga}_{1-z}\text{Al}_z\text{As}$ layer) can be 0.1 or more and 0.4 or less. Although the buffer layer of Inoue is made of $\text{Ga}_{1-z}\text{In}_z\text{As}$, it is also taught that In can be replaced with other group III elements, such as B or Al (Col.7, lines 20-23). Further, Inoue discloses that the composition of the In content is not limited and can be smaller or larger (col.6, line 55 – col.7, line 6).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to choose relative composition of the element as recited in the claim, in order to achieve maximum absorption of the distortion cause as a result of the lattice mismatch.

Regarding claims 14 and 15, Udagawa teaches a superlattice buffer layers (col. 4, lines 19-23).

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

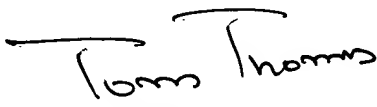
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmi
June 16, 2003


TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800